What Is Claimed Is:

1. A reconfigurable hardware apparatus for performing computational operations in one of a downsampling mode and a non-downsampling mode, comprising:

a plurality of adders, each of the plurality of adders including at least two inputs and one output;

a plurality of multipliers, each of the plurality of multipliers including at least two inputs and one output;

a switching fabric for switching between a downsampling mode of operation and a non-downsampling mode of operation, wherein the switching fabric provides for a configuration of the inputs and outputs of the adders with respect to the inputs and outputs of the multipliers; and,

a control logic block for controlling the switching fabric.

2. The hardware apparatus according to claim 1, wherein in the non-downsampling mode, the switching apparatus configures the multipliers and adders to include a plurality of MAAC kernels.

3. The hardware apparatus according to claim 1, wherein in the downsampling mode, the switching apparatus configures the multipliers and adders to include a plurality of MAAC kernels and at least one AMAAC kernel.

4. The hardware apparatus according to claim 2, wherein the MAAC kernel includes a multiplier block, an adder block and a register block, wherein an output of the multiplier block is coupled to an input of the adder block, an output of the adder block is coupled to an input of the register block and an output of the register block is coupled to a second input of the adder block and the adder block receives at its second input an additional addend.

5. The hardware apparatus according to claim 3, wherein the AMAAC kernel includes a multiplier block, a first adder block, a second adder block and a register block,wherein the first adder block receives two inputs (e(i) and a(i)) and an output of the first adder block is coupled to a first input of the multiplier block, the multiplier

block receiving a second input (b(i)) and an output of the multiplier block coupled to a first input of the second adder block, the second adder block receiving a second input (c(i)) and an output of the second adder block is coupled to an input of the register block, an output of the register block coupled to a third input of the second adder block.

6. The hardware apparatus according to claim 1, wherein the computational operations include transformations.

7. The hardware apparatus according to claim 6, wherein the transformations include an inverse Discrete Cosine Transform (IDCT).

8. The hardware apparatus according to claim 7, wherein in the non-downsampling mode, an eight-point IDCT is computed utilizing the following expression:

$$\begin{bmatrix} x_0 \\ x_1 \\ x_2 \\ x_3 \end{bmatrix} = \frac{1}{2}A' \begin{bmatrix} y_0 \\ y_4 \\ y_2 \\ y_6 \end{bmatrix} + \frac{1}{2}B' \begin{bmatrix} y_1 \\ y_5 \\ y_3 \\ y_7 \end{bmatrix} \qquad \begin{bmatrix} x_7 \\ x_6 \\ x_5 \\ x_4 \end{bmatrix} = \frac{1}{2}A' \begin{bmatrix} y_0 \\ y_4 \\ y_2 \\ y_6 \end{bmatrix} - \frac{1}{2}B' \begin{bmatrix} y_1 \\ y_5 \\ y_3 \\ y_7 \end{bmatrix}$$

where:

$$A' = \begin{bmatrix} 1 & 1 & c'(2) & c'(6) \\ 1 & -1 & c'(6) & -c'(2) \\ 1 & -1 & -c'(6) & c'(2) \\ 1 & 1 & -c'(2) & -c'(6) \end{bmatrix} \qquad B = \begin{bmatrix} c'(1) & c'(5) & c'(3) & c'(7) \\ c'(3) & -c'(1) & -c'(7) & -c'(5) \\ c'(5) & c'(7) & -c'(1) & c'(3) \\ c'(7) & c'(3) & -c'(5) & -c'(1) \end{bmatrix}$$

9. The hardware apparatus according to claim 7, wherein in the downsampling mode, a 2:1 downsampling of an eight-point IDCT is computed utilizing the following expression:

$$\begin{bmatrix} x_0 \\ x_1 \\ x_2 \\ x_3 \end{bmatrix} = c(4) \begin{bmatrix} y_0 - y_7 + y_2 - y_5 + c'(2) * y_1 - c'(2) * y_6 + c'(6) * y_3 - c'6 * y_4 \\ y_0 - y_7 - y_2 + y_5 + c'(6) * y_1 - c'(6) * y_6 - c'(2) * y_3 + c'(2) * y_4 \\ y_0 - y_7 - y_2 + y_5 - c'(6) * y_1 + c'(6) * y_6 + c'(2) * y_3 - c'(2) * y_4 \\ y_0 - y_7 + y_2 - y_5 - c'(2) * y_1 + c'(2) * y_6 - c'(6) * y_3 + c'(6) * y_4 \end{bmatrix}$$

10. A hardware apparatus for computing an IDCT in one of a downsampling mode and a non-downsampling mode comprising:

a data loader block;

a plurality of MAAC kernels; and

at least one AMAAC kernel.

11. The hardware apparatus according to claim 10, wherein each MAAC kernel includes a multiplier block, an adder block and a register block, wherein an output of the multiplier block is coupled to an input of the adder block, an output of the adder block is coupled to an input of the register block and an output of the register block is coupled to a second input of the adder block and the adder block receives at its second input an additional addend.

12. The hardware apparatus according to claim 10, wherein each AMAAC kernel includes a multiplier block, a first adder block, a second adder block and a register block, wherein the first adder block receives two inputs (e(i) and a(i)) and an output of the first adder block is coupled to a first input of the multiplier block, the multiplier block receiving a second input (b(i)) and an output of the multiplier block coupled to a first input of the second adder block, the second adder block receiving a second input (c(i)) and an output of the second adder block is coupled to an input of the register block, an output of the register block coupled to a third input of the second adder block.

13. A system for performing downsampling computations:

at least one AMAAC kernel, wherein each AMAAC kernel includes:

a multiplier block;

a first adder block;

a second adder block;

a register block;

wherein the first adder block receives two inputs (e(i) and a(i)) and an output of the first adder block is coupled to a first input of the multiplier block, the multiplier block receiving a second input (b(i)) and an output of the multiplier block coupled to a first input of the second adder block, the second adder block receiving a second input (c(i)) and an output of the second adder block is coupled to an input of the register block, an output of the register block coupled to a third input of the second adder block;

at least one MAAC kernel, wherein each MAAC kernel includes:

a multiplier block;

an adder block;

a register block;

wherein an output of the multiplier block is coupled to a first input of the adder block, an output of the adder block is coupled to an input of the register block and an output of the register block is coupled to a second input of the adder block, the adder block receiving a third input.

14. The system according to claim 13, wherein the downsampling computations are performed as part of a video decoding system.

15. The system according to claim 13, wherein the downsampling operations are performed in conjunction with an IDCT process.

16. A digital signal processor wherein the digital signal processor includes:

at least one MAAC kernel; and,

at least one AMAAC kernel.

17. The digital signal processor according to claim 16, wherein the digital signal processor includes instructions for controlling the at least one MAAC kernel.

18. The digital signal processor according to claim 16, wherein the digital signal processor includes instructions for controlling the at least one AMAAC kernel.